I CLAIM:

1. A structure comprising:

a varactor comprising (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a gate dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the plate and body regions being of opposite conductivity types and meeting each other to form a p-n junction, the plate electrode being at a plate-to-body voltage relative to the body electrode, the gate electrode being at a gate-to-body voltage relative to the body electrode, an inversion layer occurring in the body region along the gate dielectric layer below the gate electrode, the inversion layer comprising multiple variably appearing inversion portions respectively characterized by corresponding zero-point threshold voltages of like sign, each inversion portion largely appearing/ disappearing when the gate-to-body voltage passes through the corresponding zero-point threshold voltage with the plate-to-body voltage at zero, each inversion portion meeting the plate region or/and being continuous with another inversion portion whose zero-point threshold voltage is of lower magnitude than the zero-point threshold voltage of that inversion portion; and

further electronic circuitry having a capacitance signal path for receiving the varactor to enable the further circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

2. A structure as in Claim 1 wherein the inversion portions comprise at least two inversion portions which, when present, meet the plate region.

3. A structure as in Claim 2 wherein the inversion portions comprise a first inversion portion and a second inversion portion whose zero-point threshold voltage is of greater magnitude than the zero-point threshold voltage of the first inversion portion, the first inversion portion extending between the second inversion portion and the plate region when both of the first and second inversion portions are present such that the second inversion portion is spaced apart from the plate region.

4. A structure as in Claim 3 wherein the inversion portions include a third inversion portion whose zero-point threshold voltage is of greater magnitude than the zero-point threshold voltage of the other two inversion portions, the second inversion portion extending between the first inversion portion and the third inversion portion when the first, second, and third inversion portions are present such that the third inversion portion is also spaced apart from the plate region.

5. A structure as in Claim 3 wherein the inversion portions include a third inversion portion that meets the plate region.

6. A structure as in Claim 1 wherein the gate dielectric layer comprises multiple gate dielectric portions of different respective thicknesses, each gate dielectric portion situated above at least where a different corresponding of the inversion portions occurs.

7. A structure as in Claim 6 wherein each gate dielectric portion extends to a location above the plate region or/and is continuous with a gate dielectric portion thinner than that gate dielectric portion.

8. A structure as in Claim 7 wherein the gate dielectric portions comprise a first gate dielectric portion and a second gate dielectric portion thicker than the first gate dielectric portion, the first gate dielectric portion extending between the second gate dielectric portion and a location above the plate region such that the second gate dielectric portion is spaced laterally apart from the plate region.

9. A structure as in Claim 7 wherein each of at least two of the gate dielectric portions extend to a location above the plate region.

10. A structure as in Claim 1 wherein a surface depletion region of the body region extends along the gate dielectric layer below the gate electrode, the surface depletion region comprising multiple surface depletion portions of different respective average net dopant concentrations, each surface depletion portion situated below where a different corresponding one of the inversion portions occurs.

11. A structure as in Claim 10 wherein each surface depletion portion meets the plate region or/and is continuous with a surface depletion portion more lightly doped than that surface depletion portion.

12. A structure as in Claim 11 wherein the surface depletion portions comprise a first surface depletion portion and a second surface depletion portion more heavily doped than the first surface depletion portion, the first surface depletion portion extending between the second surface depletion portion and the plate region such that the second surface depletion portion is spaced apart from the plate region.

13. A structure as in Claim 1 wherein the gate electrode comprises multiple gate electrode portions of semiconductor material, each gate electrode portion situated above at least where a different corresponding one of the inversion portions occurs, each gate electrode portion being of a different conductivity type or/and a different average net dopant concentration than each other gate electrode portion.

14. A structure as in Claim 13 wherein the gate electrode portions comprise first and second gate electrode portions of the same conductivity type and different average net dopant concentrations.

15. A structure as in Claim 14 wherein the first and second gate electrode portions are of opposite conductivity type to the body region, the first gate electrode portion being more lightly doped than the second gate electrode portion and extending between the second gate electrode portion and a location above the plate region such that the second gate electrode portion is spaced laterally apart from the plate region.

16. A structure as in Claim 14 wherein the first and second gate electrode portions are of the same conductivity type as the body region, the first gate electrode portion being more heavily doped than the second gate electrode portion and extending between the second gate electrode portion and a location above the plate region such that the second gate electrode portion is spaced laterally apart from the plate region.

17. A structure as in Claim 13 wherein the gate electrode portions comprise (a) a first gate electrode portion of opposite conductivity type to the body region and (b) a second gate electrode portion of the same conductivity type as the body region.

18. A structure as in Claim 17 wherein the first gate electrode portion extends between the second gate electrode portion and a location above the plate region such that the second gate electrode portion is spaced laterally apart from the plate region.

19. A structure as in Claim 17 wherein the gate electrode includes a metal-containing layer for electrically shorting the first and second gate electrode portions to each other.

20. A structure as in Claim 13 wherein the semiconductor material of the gate electrode portions comprises non-monocrystalline semiconductor material.

21. A structure as in Claim 20 wherein the non-monocrystalline semiconductor material comprises polycrystalline semiconductor material.

22. A structure as in Claim 1 wherein:

the gate dielectric layer comprises a first gate dielectric portion and a second gate dielectric portion thicker than the first gate dielectric portion, each gate dielectric portion situated above at least where a different corresponding one of the inversion portions occurs; and

the gate electrode comprises (a) a first gate electrode portion of semiconductor material of opposite conductivity type to the body region and (b) a second gate electrode portion of semiconductor material of the same conductivity type as the body region, the first gate electrode portion overlying the first and second gate dielectric portions, the second gate electrode portion situated above at least where a further corresponding one of the inversion portions occurs.

23. A structure as in Claim 22 wherein:

the first gate dielectric portion extends between the second gate dielectric portion and a location above the plate region such that the second gate dielectric portion is spaced laterally apart from the plate region; and

the first gate electrode portion extends between the second gate electrode portion and a location above the plate region such that the second gate electrode portion is spaced laterally apart from the plate region.

24. A structure as in Claim 22 wherein the gate dielectric layer includes a third gate dielectric portion of approximately the same thickness as the first gate dielectric portion, the second gate electrode portion overlying the third gate dielectric portion.

25. A structure as in Claim 22 wherein the gate electrode includes a metal-containing layer for electrically shorting the first and second gate electrode portions to each other.

26. A structure as in Claim 22 wherein the semiconductor material of the gate electrode portions comprises non-monocrystalline semiconductor material.

27. A structure as in Claim 26 wherein the non-monocrystalline semiconductor material comprises polycrystalline semiconductor material.

28. A structure as in Claim 1 wherein the gate electrode comprises multiple gate electrode portions of metal, each gate electrode portion situated above at least where a different corresponding one of the inversion portions occurs, each gate electrode portion being of a different work function than each other gate electrode portion.

29. A structure as in Claim 1 wherein the further circuitry comprises at least one additional region of the semiconductor body.

30. A structure as in Claim 1 wherein the further circuitry comprises an inductor.

31. A structure as in Claim 1 wherein:

a surface depletion region of the body region extends along the gate dielectric layer below the gate electrode; and

a body contact portion of the body region is contacted by the body electrode, is spaced apart from the surface depletion region, and is more heavily doped than the surface depletion region.

32. A structure as in Claim 1 wherein the further circuitry maintains the gate-to-body voltage approximately constant as the plate-to-body voltage is varied.

33. A structure as in Claim 1 wherein:

the varactor has a capacitance as measured between the plate and body electrodes; and

the structure includes an input circuit responsive to an input signal for generating the plate-to-body voltage such that the varactor's capacitance varies approximately linearly with the input signal.

34. A structure comprising:

a varactor comprising (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a gate dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the plate and body regions being of opposite conductivity types and meeting each other to form a p-n junction, the gate dielectric layer comprising multiple gate dielectric portions of different respective thicknesses, each gate dielectric portion extending to a location above the plate region or/and being continuous with a gate dielectric portion thinner than that gate dielectric portion; and

further electronic circuitry having a capacitance signal path for receiving the varactor to enable the further circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

35. A structure as in Claim 34 wherein the gate dielectric portions comprise a first gate dielectric portion and a second gate dielectric portion thicker than the first gate dielectric portion, the first gate dielectric portion extending between the second gate dielectric portion and a location above the plate region such that the second gate dielectric portion is spaced laterally apart from the plate region.

36. A structure as in Claim 35 wherein the gate dielectric portions comprise a third gate dielectric portion that meets the plate region.

37. A structure as in Claim 34 wherein each of at least two of the gate dielectric portions extend to a location above the plate region.

38. A structure as in Claim 34 wherein:

a surface depletion region of the body region extends along the gate dielectric layer below the gate electrode; and

a body contact portion of the body region is contacted by the body electrode, is spaced apart from the surface depletion region, and is more heavily doped than the surface depletion region.

39. A structure comprising:

a varactor comprising (a) a plate region and body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a gate dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the plate and body regions being of opposite conductivity types and meeting each other to form a p-n junction, a surface depletion region of the body region extending along the gate dielectric layer below the gate electrode, the surface depletion region comprising multiple surface depletion portions of different respective average net dopant concentrations, each surface depletion portion meeting the plate region or/and being continuous with a surface depletion portion more lightly doped than that surface depletion portion; and

further electronic circuitry having a capacitance signal path for receiving the varactor to enable the further circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

40. A structure as in Claim 39 wherein the surface depletion portions comprise a first surface depletion portion and a second surface depletion portion more heavily doped than the first surface depletion portion, the first surface depletion portion extending between the second surface depletion portion and the plate region such that the second surface depletion portion is spaced apart from the plate region.

41. A structure as in Claim 39 wherein:

a surface depletion region of the body region extends along the gate dielectric layer below the gate electrode; and

a body contact portion of the body region is contacted by the body electrode, is spaced apart from the surface depletion region, and is more heavily doped than the surface depletion region.

42. A structure comprising:

a varactor comprising (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a gate dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the gate dielectric layer at least one where the gate dielectric layer contacts material of the body region, the plate and body regions being of opposite conductivity types and meeting each other to form a p-n junction, the gate electrode comprising multiple gate electrode portions of semiconductor material, each gate electrode portion being of different conductivity type or/and different average net dopant concentration than each other gate electrode portion; and

further electronic circuitry having a capacitance signal path for receiving the varactor to enable the further circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

43. A structure as in Claim 42 wherein the gate electrode portions comprise first and second gate electrode portions of the same conductivity type and different average net dopant concentrations.

44. A structure as in Claim 42 wherein the gate electrode portions comprise (a) a first gate electrode portion of opposite conductivity type to the body region and (b) a second gate electrode portion of the same conductivity type as the body region.

45. A structure as in Claim 44 wherein the first gate electrode portion extends between the second gate electrode portion and a location above the plate region such that the second gate electrode portion is spaced laterally apart from the plate region.

46. A structure as in Claim 44 wherein the gate electrode includes a metal-containing layer for electrically shorting the first and second gate electrode portions to each other.

47. A structure as in Claim 42 wherein:

the gate dielectric layer comprises a first gate dielectric portion and a second gate dielectric portion thicker than the first gate dielectric portion, each gate dielectric portion situated above at least where a different corresponding one of the inversion portions occurs; and

the gate electrode portions comprise (a) a first gate electrode portion of opposite conductivity type to the body region and (b) a second gate electrode portion of the same conductivity type as the body region, the first gate electrode portion overlying the first and second gate dielectric portions, the second gate electrode portion situated above at least where a further corresponding one of the inversion portions occurs.

48. A structure as in Claim 47 wherein:

the first gate dielectric portion extends between the second gate dielectric portion and a location above the plate region such that the second gate dielectric portion is spaced laterally apart from the plate region; and

the first gate electrode portion extends between the second gate electrode portion and a location above the plate region such that the second gate electrode portion is spaced laterally apart from the plate region.

49. A structure as in Claim 47 wherein the gate dielectric layer includes a third gate dielectric portion of approximately the same thickness as the first gate dielectric portion, the second gate electrode portion overlying the third gate dielectric portion.

50. A structure as in Claim 47 wherein the gate electrode includes a metal-containing layer for electrically shorting the first and second gate electrode portions to each other.

51. A structure as in Claim 42 wherein the semiconductor material of the gate electrode comprises non-monocrystalline semiconductor material.

52. A structure as in Claim 51 wherein the non-monocrystalline semiconductor material comprises polycrystalline semiconductor material.

53. A structure comprising:

a plate region and a body region of the semiconductor body, the plate and body regions being of opposite conductivity types and meeting each other to form a p-n junction;

a gate dielectric layer situated over the semiconductor body and contacting the body region;

a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the gate electrode comprising multiple gate electrode portions of semiconductor material, each gate electrode portion being of different conductivity type or/and different average net dopant concentrations than each other gate electrode portion.

54. A structure as in Claim 53 wherein the gate electrode portions comprise first and second gate electrode portions of the same conductivity type and different average net dopant concentrations.

55. A structure as in Claim 54 wherein the first and second gate electrode portions are of opposite conductivity type to the body region, the first gate electrode portion being more lightly doped than the second gate electrode portion and extending between the second gate electrode portion and a location above the plate region such that the second gate electrode portion is spaced laterally apart from the plate region.

56. A structure as in Claim 54 wherein the first and second gate electrode portions are of the same conductivity type as the body region, the first gate electrode portion being more heavily doped than the second gate electrode portion and extending between the second gate electrode portion and a location above the plate region such that the second gate electrode portion is spaced laterally apart from the plate region.

57. A structure as in Claim 53 wherein the gate electrode portions comprise (a) a first gate electrode portion of opposite conductivity type to the body region and (b) a second gate electrode portion of the conductivity type as the body region.

58. A structure as in Claim 57 wherein the first gate electrode portion extends between the second gate electrode portion and a location above the plate region such that the second gate electrode portion is spaced laterally apart from the plate region.

59. A structure as in Claim 53 wherein:

the gate dielectric layer comprises a first gate dielectric portion and a second gate dielectric portion thicker than the first gate dielectric portion, each gate dielectric portion situated above at least where a different corresponding one of the inversion portions occurs; and

the gate electrode portions comprise (a) a first gate electrode portion of opposite conductivity type to the body region and (b) a second gate electrode portion of the same conductivity type as the body region, the first gate electrode portion overlying the first and second gate dielectric portions, the second gate electrode portion situated above at least where a further corresponding one of the inversion portions occurs.

60. A structure as in Claim 59 wherein:

the first gate dielectric portion extends between the second gate dielectric portion and a location above the plate region such that the second gate dielectric portion is spaced laterally apart from the plate region; and

the first gate electrode portion extends between the second gate electrode portion and a location above the plate region such that the second gate electrode portion is spaced laterally apart from the plate region.

61. A method comprising:

selecting a varactor that comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and body electrode respectively connected to the plate and body regions, (c) a gate dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the plate and body regions being of opposite conductivity types, meeting each other to form a p-n junction, and extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, the varactor having a minimum capacitance dependent on the plate area, an inversion layer that meets the plate region occurring in the body region

and occupying a lateral inversion area along the primary surface, the inversion area reaching a maximum value when the inversion layer is fully present, the varactor having a maximum capacitance dependent on the maximum inversion area in common with the plate area, the plate electrode being at a plate-to-body voltage relative to the body electrode, the gate electrode being at a gate-to-body voltage relative to the body electrode, the inversion layer comprising multiple variably appearing inversion portions respectively characterized by corresponding different zero-point threshold voltages of like sign, each inversion portion appearing/disappearing when the gate-to-body voltage passes through the corresponding zero-point threshold voltage with the plate-to-body voltage at zero, each inversion portion meeting the plate region or/and being continuous with the another inversion portion whose zero-point threshold voltage is of lower magnitude than the zero-point threshold voltage of that inversion portion; and

adjusting the plate and maximum inversion areas to control the maximum and minimum capacitances of the varactor.

62. A method as in Claim 61 wherein the minimum capacitance is approximately proportional to the plate area, and the maximum capacitance is approximately proportional to an accumulative combination of the plate and maximum inversion areas.

63. A method as in Claim 61 wherein the adjusting act involves adjusting the ratio of the maximum inversion area to the plate area in order to achieve at least a specified value of the ratio of the maximum capacitance to the minimum capacitance.

64. A method as in Claim 61 further including maintaining the gate-to-body voltage approximately constant as the plate-to-body voltage is varied.

65. A method as in Claim 61 wherein the gate dielectric layer comprises multiple gate dielectric portions of different respective thicknesses, each gate dielectric portion situated above at least where a different corresponding of the inversion portions occurs.

66. A method as in Claim 61 wherein a surface depletion region of the body region extends along the gate dielectric layer below the gate electrode, the surface depletion region comprising multiple surface depletion portions of different respective average net dopant

concentrations, each surface depletion portion situated below where a different corresponding one of the inversion portions occurs.

67. A method as in Claim 61 wherein the gate electrode comprises multiple gate electrode portions of semiconductor material, each gate electrode portion situated above at least where a different corresponding one of the inversion portions occurs, each gate electrode portion being of a different conductivity type or/and a different average net dopant concentration than each other gate electrode portion.

68. A method as in Claim 61 wherein:

the gate dielectric layer comprises a first gate dielectric portion and second gate dielectric portion thicker than the first gate dielectric portion, each gate dielectric portion situated above at least where a different corresponding one of the inversion portions occurs; and

the gate electrode comprises (a) a first gate electrode portion of semiconductor material of opposite conductivity type to the body region and (b) a second gate electrode portion of semiconductor material of the same conductivity type as the body region, the first gate electrode portion overlying the first and second gate dielectric portions, the second gate electrode portion situated above at least where a further corresponding one of the inversion portions occurs.